CLAIMS

1. A limiter comprising:

a transistor including a floating gate and a control gate,

wherein the floating gate and the control gate of the transistor overlap each other with an insulating film interposed therebetween;

a drain of the transistor is connected to the control gate; and

the drain and the control gate are connected to an input terminal and an output terminal.

2. A limiter comprising:

a transistor including a floating gate and a control gate,

wherein the floating gate and the control gate of the transistor overlap each other with an insulating film interposed therebetween;

a drain of the transistor is connected to the control gate; and

a source of the transistor is connected to an input terminal and an output terminal.

3. A limiter comprising:

a plurality of transistors each includes a floating gate and a control gate,

wherein the floating gate and the control gate of each of the transistors overlap each other with an insulating film interposed therebetween;

a drain of each of the transistors is connected to the control gate;

the plurality of transistors are connected in series so as to have the same forward current direction; and

the drain and the control gate of one of the transistors, which is connected at the end, are connected to an input terminal and an output terminal.

4. A limiter comprising:

a plurality of transistors each includes a floating gate and a control gate,,

wherein the floating gate and the control gate of each of the transistors overlap each other with an insulating film interposed therebetween;

a drain of each of the transistors is connected to the control gate;

the plurality of transistors are connected in series so as to have the same forward current direction; and

a source of one of the transistors, which is connected at the end, is connected to an input terminal and an output terminal.

5. A limiter comprising:

a first transistor, and

a second transistor,

wherein a floating gate and a control gate of the first transistor overlap each other with an insulating film interposed therebetween;

a drain of the first transistor is connected to the control gate of the first transistor;

a drain of the second transistor is connected to a gate of the second transistor;

the first transistor and the second transistor are connected in series so as to have the same forward current direction; and

the drain of the second transistor and the control gate are connected to an input terminal and an output terminal.

6. A limiter comprising:

a first transistor, and

a second transistor,

wherein a floating gate and a control gate of the first transistor overlap each other with an insulating film interposed therebetween;

a drain of the first transistor is connected to the control gate of the first transistor;

a drain of the second transistor is connected to a gate of the second

transistor;

the first transistor and the second transistor are connected in series so as to have the same forward current direction; and

a source of the second transistor is connected to an input terminal and an output terminal.

7. The limiter according to any one of claims 1 to 6 further comprising a connecting terminal for controlling the amount of charge accumulated in the floating gate.

8. The limiter according to any one of claims 1 to 6 further comprising a resistor.

9. The limiter according to any one of claims 1 to 6, wherein the transistor is a thin film transistor.

10. A semiconductor device comprising:

an integrated circuit, and

an antenna connected to the integrated circuit,

wherein the integrated circuit includes a limiter;

the limiter includes a transistor;

a floating gate and a control gate of the transistor overlap each other with an insulating film interposed therebetween;

a drain of the transistor is connected to the control gate.

11. A semiconductor device comprising an integrated circuit and an antenna connected to the integrated circuit,

wherein the integrated circuit includes a limiter, a pulse generation circuit for controlling a limit voltage of the limiter, and a booster circuit for supplying a power supply voltage to the pulse generation circuit;

the limiter includes a transistor;

a floating gate and a control gate of the transistor overlap each other with an insulating film interposed therebetween;

a drain of the transistor is connected to the control gate; and

the drain and the control gate are connected to one terminal of the resistor.

12. The semiconductor device according to claim 10 or 11, wherein the transistor is a thin film transistor.

13. The semiconductor device according to claim 10 or 11 further comprising a resistor.